In the Abstract

Please amend the Abstract as follows:

An architecture for a highly configurable and scalable microprocessor architecture designed for exploiting instruction level parallelism in specific application code. ~~It consists of a number of execution units with configurable connectivity between them and a means to copy data through execution units under software control.~~ Certain functional units may have to communicate data that are not directly connected. To support this certain functional units are able to copy data from their input operands to their outputs. That way data can be transported around the functional units as required using copies through functional units.